

On page 36, line 10, after "registers" insert --173--.

On page 36, line 12, after "registers" insert --172--.

On page 36, line 15, after "register" insert --171--.

On page 38, line 23, after the second occurrence of "register" insert --171--.

On page 38, line 25, after "register" insert --173--.

On page 39, line 6, after "register" insert --173--.

On page 54, line 13, delete "70" and substitute --69--.

IN THE DRAWING:

Please add new Figure 16, attached hereto.

IN THE CLAIMS:

Kindly amend the following claims:

- 1 151. (Amended) A synchronous semiconductor memory device
- 2 having at least one memory section including a plurality of memory
- 3 cells, the memory device comprising:
- 4 clock receiver circuitry to receive an external clock signal;
- 5 a register which stores a value which is representative of a
- 6 delay time after which the memory device responds to a read
- 7 request; and

8
B 9
10 a plurality of output drivers to output data after [in
accordance with] the delay time transpires and synchronously with
respect to the external clock signal.

3
1 153. (Amended) The memory device of claim ~~152~~ wherein the
2 plurality of output drivers output data in response to a rising
3 edge of the external [internal] clock signal.

1 157. (Amended) A synchronous semiconductor memory device
2 having at least one memory section including a plurality of memory
3 cells, the memory device comprising:
4 clock receiver circuitry to receive an external clock signal;
5 at least one register to store a value which is representative
6 of a delay time; and
7 wherein in response to a read request, the memory device
8 outputs data after [in accordance with] the delay time transpires
9 and synchronously with respect to the external clock signal.

15
B 1 161. (Amended) The memory device of claim ~~157~~ wherein the
2 memory device, in response to a control register access [set
3 register request], stores a value in the at least one register.

23
B 1 163. (Amended) A method of controlling [operating] a
2 synchronous [semiconductor] memory device having at least one

memory section including a plurality of memory cells and a register for storing a value which is representative of a time delay after which the memory device responds to a read request, the method comprising:

issuing a read request to the memory device; and
receiving data from [wherein] the memory device, in response to the read request, wherein the memory device outputs the data after [on a bus in accordance with] the time delay transpires and synchronously with respect to an external clock signal.

137
24
23
164. (Amended) The method of claim 163 further including issuing a control register access [set register request], wherein, in response to the control register access [set register request], the memory device stores the value in the register.

25
24
165. (Amended) The method of claim 164 wherein the control register access [set register request] and the value are provided to the memory device in a single request packet.

27
23
167. (Amended) The method of claim 163 further including [the steps of]:

138
168. (Amended) The method of claim 167 further including [the steps of]:
initializing the register in the memory device by issuing a control register access [set register request] on the bus; and providing the value which is representative of the time delay.

28 23
168. (Amended) The method of claim 163 further including [the
step of] identifying the memory device on the bus using a device
identification code.

Kindly ADD the following claims:

1 -- ²173. The synchronous memory device of claim ¹151 wherein
2 the value is representative of a number of clock cycles of the
3 external clock.

1 ⁸174. The memory device of claim ⁷173 wherein the value which is
2 representative of the delay time is stored in the register after
3 power is applied to the device.

1 ⁹175. The memory device of claim ⁸174 further including:
2 a delay locked loop, coupled to the clock receiver circuitry,
3 to generate an internal clock signal using at least the external
4 clock signal; and

5 wherein the plurality of output drivers output data in
6 response to the internal clock signal.

1 ¹⁰176. The memory device of claim ⁹174 wherein the value stored
2 in the register is representative of one of a plurality of
3 different delay times.

75

1 ¹⁷~~177~~. The synchronous memory device of claim ¹¹~~157~~ wherein the
2 value is representative of a number of clock cycles of the external
3 clock signal..

1 ¹⁸~~178~~. The memory device of claim ¹⁷~~177~~ wherein the value which is
2 representative of the delay time is stored in the register after
3 power is applied to the device.

1 ¹⁹~~179~~. The memory device of claim ¹⁷~~177~~ further including:
2 a delay locked loop, coupled to the clock receiver circuitry,
3 to generate an internal clock signal using at least the external
4 clock signal; and
5 wherein the plurality of output drivers output data in
6 response to the internal clock signal.

1 ²⁰~~180~~. The memory device of claim ¹⁷~~177~~ wherein the memory device
2 outputs data in response to a rising edge of the external clock
3 signal.

1 ²¹~~181~~. The memory device of claim ²⁰~~180~~ further including:
2 clock generation circuitry, coupled to the clock receiver
3 circuitry, to generate an internal clock signal; and

4 an output driver, coupled to the internal clock generation
5 circuitry, to output the data in response to the internal clock
6 signal.

1 ²²182. The memory device of claim ²⁴181 wherein the output driver
2 outputs data in response to a rising edge of the internal clock
3 signal.

1 ²³183. The method of claim ²³163 wherein the external clock signal
2 has a fixed frequency.

1 ³⁴184. A synchronous semiconductor memory device having at least
2 one memory section including a plurality of memory cells, the
3 memory device comprising:

4 clock receiver circuitry to receive an external clock signal;
5 a register which stores a value which is representative of a
6 number of cycles of the external clock signal to transpire after
7 which the memory device responds to receiving a request to provide
8 data; and

9 a plurality of output drivers to output data in response to
10 receiving a request to provide data, wherein the data is provided
11 after the number of cycles of the external clock signal represented
12 by the value have transpired.

35
1 185. The memory device of claim 184 wherein the plurality of
2 output drivers output data synchronously with respect to a
3 transition of the external clock signal.

34
1 186. The memory device of claim 184 further including input
2 receiver circuitry, coupled to the bus, to receive the request to
3 provide data, wherein the request to provide data is sampled from
4 the bus synchronously with respect to the external clock signal.

37
1 187. The memory device of claim 186 wherein the input receiver
2 circuitry further includes a first input latch coupled to the bus,
3 wherein the first input latch samples a first information bit
4 synchronously with respect to a rising edge of the external clock
5 signal.

38
1 188. The memory device of claim 187 wherein the input receiver
2 circuitry further includes a second input latch coupled to the bus,
3 wherein the second input latch samples a second information bit
4 synchronously with respect to a falling edge of the external clock
5 signal.

39
1 189. The memory system of claim 188 the first and second
2 information bits are included in the request to provide data, and